1 **CIRCUIT DESIGN**
2 .Optimization (e.g., redundancy, compaction)
3 .Translation (e.g., conversion, equivalence)
4 .Testing or evaluating
5 ..Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width)
6 ...Timing analysis (e.g., delay time, path delay, latch timing)
7 .Partitioning (e.g., function block, ordering constraint)
8 .Floorplanning
9 ..Detailed placement (i.e., iterative improvement)
10 ..Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance)
11 ..Layout editor (e.g., updating)
12 .Routing (e.g., routing map, netlisting)
13 ..Global routing (e.g., shortest path, dead space, or duplicate trace elimination)
14 ..Detailed routing (e.g., channel routing, switch box routing)
15 ..PCB wiring
16 ..PLA, PLD, FPGA, OR MCM
17 .Programmable integrated circuit (e.g., basic cell, standard cell, macrocell)
18 .Logical circuit synthesizer
19 **DESIGN OF SEMICONDUCTOR MASK**
20 .Mesh generation
21 .Pattern exposure

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

APPLICATIONS (364/400)

FOR 489 .Circuit design and analysis (364/489)
FOR 490 ..Integrated (364/490)
FOR 491 ...Layout (364/491)